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09/988,593	11/20/2001	Shigenobu Maeda	50099-180	8927

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600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

PHAM, THANH V

ART UNIT	PAPER NUMBER
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2823

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 15

Application Number: 09/988,593
Filing Date: November 20, 2001
Appellant(s): MAEDA ET AL.

Scott D. Paul
For Appellant

EXAMINER'S ANSWER

MAILED
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GROUP 2800

This is in response to the appeal brief filed 11/04/03.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

(7) *Grouping of Claims*

The rejection of claims 1-9 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,410,369

Flaker et al.

6-2002

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-9 are rejected under 35 U.S.C. 102(a) as being anticipated by Flaker et al. U.S. Patent No. 6,410,369 B1.

The Flaker et al. reference, in its abstract and the detailed description, discloses a semiconductor device having an SOI structure formed by a semiconductor substrate, an embedded insulating layer 48 and a first conductivity (p-)type SOI layer 46, comprising: a plurality of element forming regions 54, each formed with prescribed elements (fig.'s 8, 10 and 12); an isolation film 40 (fig. 10B) provided in an upper layer part of said SOI layer for isolating said plurality of element forming regions from each other; a first conductivity semiconductor region (*body link*, fig. 10B) provided under said isolation film 40 as part of said SOI layer, said first conductivity body link semiconductor region being formed in contact with at least one of said plurality of element forming regions; and a p-type body region provided in said SOI layer and capable of being externally fixed in electric potential (fig. 8), said body region being in contact with said semiconductor region, wherein said body link semiconductor region at least partially has a first conductivity type impurity region not mixed with an impurity of a second conductivity type different from said first conductivity type but doped by only an impurity of said first conductivity type and said first conductivity type semiconductor region is formed in a region reaching said at least one element forming region from said body

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region (col. 3, line 65 – col. 4, line 2). Re claim 5, the p-body section adjacent to element 40 and the body link 32 has a larger thickness than the body link 32, fig. 10B.

The device of Flaker et al. in fig. 10B is made by a process of figs. 11-20 in which mask layers 54 and 56 are provided (figs 12-13) "where it is desired to form a selective equilibration body link" (col. 6, lines 6-7) prior to the step of high-pressure low-temperature oxidation cycle which allows "very precise control of the oxidation depth" by forming an implanted region having a depth equal to the depth of the oxide region desired (col. 6, lines 19-20). Then the oxide region 60 of fig. 13 is etched selectively to the p-type silicon (col. 6, lines 29-34) to leave the p-body and the body link without second conductivity type as shown in fig. 10B and figs. 14-20). Further, as shown in fig. 13, the sections of layer 46 underneath of the implanted regions 60 are not implanted before the oxidation step because the implanted regions 60 are converted into oxide regions 62 and the reference discloses implanting in areas not protected by layers 54 and 56. No implanted regions under layer 54 and 56.

With respect to claims 7-9, there are regions on the wafer of the reference that are not active regions and could therefore be labeled as "dummy regions". Alternatively, the recitation of claim 7 "not to function as an element" is a label or statement of intended use. Flaker discloses forming the structure of fig. 20. Although the reference discloses forming n-FETs in the region on both sides of the link which by definition includes forming n-type source/drain regions and therefore regions with both n-type and p-type impurity due to the background doping of layers 46 and incorporating the n-FET in the final circuit as active devices, the region shown in fig. 20 could perform the

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function "not to function as an element" if no wiring is formed to the n-FET. Furthermore, the region disclosed in fig. 20 could perform the function of not having n-FETs formed therein, as also encompassed by claim 7. In that case appellant is claiming the intermediate product of fig. 20. Claims 8-9 fall as a group with claim 7 as stated above in the Grouping of the claims.

(11) Response to Argument

In response to appellants' argument regarding the link between the precise control of the oxidation depth and the lack of doping of the regions under element 62, the reference discloses that the doped region 60 are oxidized indicating that the regions under oxide 62 are not doped (col. 6, lines 11-23). Appellant alleges inherency of the regions under element 60 being doped but provides no reason to believe that doping as argued is inherent. Because this statement is conclusory, and not sufficiently probative of the relevant issues, it does not create a material issue of fact on which a reasonable trier of fact could find that the statement is true.

Appellant's argument regarding "dummy regions" is addressed in the statement of the rejection above.

For the above reasons, it is believed that the rejections should be sustained.


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Respectfully submitted,

wp

Thanh V. Pham
October 6, 2004

Conferees
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